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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,095	01/23/2004	Douglas Durham	15436.163.1	8239

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EXAMINER	
PASIA, REDENTOR M	

ART UNIT	PAPER NUMBER
2616	

MAIL DATE	DELIVERY MODE
04/16/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/764,095	DURHAM ET AL.	
	Examiner	**Art Unit**	
	REDENTOR M. PASIA	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _09 January 2008_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-40_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-40_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _23 January 2004_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's amendment filed on January 9, 2008 has been entered. Claims 15, 18, 19, and 30 have been amended. No claims have been cancelled. No claims have been added. Claims 1-40 are still pending in this application, with claim 1, 6, 15, 20 and 30 being independent.

Terminal Disclaimer

1. The terminal disclaimer filed on January 09, 2008 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of Application Serial No. 10/764,218 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 4-7, 9-18, 20-21, 23-31, 33-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strong (US 2004/0049706 A1; hereinafter Strong) in view of Yu et al. (US 6,070,248; hereinafter Yu).

As to claim 1, Strong shows a method for defining a common time base suitable for use in connection with the operation of a multi-link protocol analyzer in a multi-protocol communication system (abstract; Par. 0011-0012; directed to synchronizing ports that are in a domain and more particularly to synchronizing ports in a domain that is spread across different blades, chassis, backplanes, boxes, and/or protocols; directed to starting, stopping and triggering the ports at substantially the same time within a particular domain.), the method comprising:

determining a clock frequency for each of a plurality of transmission protocols associated with the multi-protocol communication system (Par. 0029; Each port is associated with a time stamp counter that generates time stamp values. Data passing through the ports is often stamped with the time stamp value obtained from the time stamp counters; Par. 0031; the ports can often support a high data rate, the clock signal of the clock 102 is multiplied by the clock multiplier 106 and the resulting clock signal of the clock multiplier is used to drive the time stamp counters of each port of each blade; Par. 0041-0042; The clock multiplier 216 of the slave box 210 multiplies the clock signal from the master box 200 and it is the multiplied clock signal (also referred to herein as the time stamp clock) that drives the time stamp counters of the ports on the slave box 210; claim 11); and

determining a frequency of a reference clock(abstract; the master box generates a clock signal that is adjusted and distributed to the slave boxes; Par. 0041-0042), where the reference clock frequency is different from each of the communications protocol clock frequencies (Figure 1-3, each slave box has a clock multiplier that

multiplies the clock signal from the master box; as shown in Figure 2-3, the boxes are in cascade fashion, and the clock signal passed from one box to another is multiplied by a factor which makes the clock different for each of the boxes (slaves and master); Par. 0041-0042).

Even though Strong has shown that each box is associated with different protocols with corresponding frequencies (Par. 0025, 0027) and generating a respective clock signal (master and various slave) for each of the boxes (Figure 3), Strong does not specifically show that his analyzer uses the plurality of communications protocol clock frequencies as a basis for determining a frequency of a reference clock.

Yu shows the step of using the plurality of communications protocol clock frequencies as a basis for determining a frequency of a reference clock (Figure 1; col. 1, line 67 to col. 2, lines 9; generate a reference clock signal having a reference frequency for an electronic device from a base clock signal having a base frequency from a base clock signal source that is external to the electronic device. Because the base clock signal source is external to the electronic device, the base frequency of the base clock signal may vary depending on the base clock signal source.). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Strong to include the features of Yu in order to have a stable reference frequency despite possible variations in the base frequency of the base clock signal (col. 6, lines 18-21).

As to claim 2, modified Strong shows the step of selecting a reference clock frequency that is an integer multiple of each of the plurality of communications protocol

clock frequencies (Strong: Par. 0031, 0042-0043; if the clock signal from the clock 204 operates at 25 MHz and the clock multipliers multiply the clock signal by a factor of four, the time stamp counters are driven by a clock signal operating at 100 MHz.).

As to claim 4, modified Strong shows that wherein the plurality of communications protocols includes at least one of the following communications protocols: Fibre Channel (Par. 0026).

As to claim 5, modified Strong shows the step of using the reference clock as a basis to determine at least one of the following: relative timing of selected data events concerning the multi-protocol communications system (Par. 0042; multiplied clock signal is also referred to as time stamp clock).

As to claim 6, Strong shows a method of processing data events associate with a multi-protocol communications system (Par. 0017), the method comprising: transmitting a reference clock (abstract; the master box generates a clock signal that is adjusted and distributed to the slave boxes; Par. 0041-0042), the reference clock frequency being different from each of the communications protocol clock frequencies (Figure 1-3, each slave box has a clock multiplier that multiplies the clock signal from the master box; as shown in Figure 2-3, the boxes are in cascade fashion, and the clock signal passed from one box to another is multiplied by a factor which makes the clock different for each of the boxes (slaves and master); Par. 0041-0042); capturing a plurality of data events, the captured data events collectively representing a plurality of communications protocols (0011-0012; when a port is triggered, data at the port is captured and stored); and timestamping at least some of the captured data events, each timestamp being

based upon the reference clock (abstract; The clock signal thus received by the slave boxes drives a clock multiplier that in turn drives the time stamp counters of the ports in the domains across the respective boxes. The time stamps of ports within a domain are synchronized because they are driven by the clock signal from the master box; Par. 0009, 0011-12, 0042).

Even though Strong has shown that each box is associated with different protocols with corresponding frequencies (Par. 0025, 0027) and generating a respective clock signal (master and various slave) for each of the boxes (Figure 3), Strong does not specifically show that the reference clock frequency is based upona plurality of communications protocol clock frequencies.

Yu shows the step of using the plurality of communications protocol clock frequencies as a basis for determining a frequency of a reference clock (Figure 1; col. 1, line 67 to col. 2, lines 9; generate a reference clock signal having a reference frequency for an electronic device from a base clock signal having a base frequency from a base clock signal source that is external to the electronic device. Because the base clock signal source is external to the electronic device, the base frequency of the base clock signal may vary depending on the base clock signal source.). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Strong to include the features of Yu in order to have a stable reference frequency despite possible variations in the base frequency of the base clock signal (col. 6, lines 18-21).

As to claim 7, modified Strong shows that the reference clock frequency comprises a frequency that is an integer multiple of each of the plurality of communications protocol clock frequencies (Strong: Par. 0031, 0042-0043; if the clock signal from the clock 204 operates at 25 MHz and the clock multipliers multiply the clock signal by a factor of four, the time stamp counters are driven by a clock signal operating at 100 MHz.).

As to claim 9, modified Strong shows at least two of the plurality of communications protocols are unsynchronized with respect to each other (Strong: Par. 0008, 0011-0013; the ports in a particular domain are of different technologies or protocols that have inherently different characteristics.).

As to claim 10, this claim is rejected for the same reasoning as set forth in the rejection of claim 4.

As to claim 11, modified Strong shows the timestamps are assigned to captured date events using clock boundaries of the reference clock (Strong: Figure 4).

As to claim 12, this claim is rejected for the same reasoning as set forth in the rejection of claim 5.

As to claim 13, Strong shows a step of receiving the reference clock (Par. 0041-0042)

As to claim 14, Strong shows a step of generating the reference clock (Par. 0042).

As to claim 15, Strong shows a protocol analyzer (100) configured for use in connection with processing data events associated with a multi-protocol

communications system (Par. 0017), the protocol analyzer comprising: a first link analyzer configured to receive data from a first communication link (110-140; Par. 0029-0030; Data passing through the ports is often stamped with the time stamp value obtained from the time stamp counters.); and a second link analyzer in at least indirect communication with the first link analyzer and configured to receive data from a second communication link (Figure 1-2), each of the first and second link analyzers also being configured to receive and transmit a trigger and a reference clock (Par. 0041-0043; The clock signal delivered to the box 220 is multiplied by the clock multiplier 228 and the multiplied clock signal from the clock multiplier drives the time stamp counters of the slave box 220.), and each of the first and second link analyzers further being configured to timestamp data in association with the reference clock (Figure 2; abstract; master box generates a clock signal that is adjusted and distributed to the slave boxes. The clock signal thus received by the slave boxes drives a clock multiplier that in turn drives the time stamp counters of the ports in the domains across the respective boxes. The time stamps of ports within a domain are synchronized because they are driven by the clock signal from the master box; Par. 0033-0034, 0042-0043), the reference clock being different from each of the communications protocol clock frequencies (Figure 1-3, each slave box has a clock multiplier that multiplies the clock signal from the master box; as shown in Figure 2-3, the boxes are in cascade fashion, and the clock signal passed from one box to another is multiplied by a factor which makes the clock different for each of the boxes (slaves and master); Par. 0041-0042).

Even though Strong has shown that each box is associated with different protocols with corresponding frequencies (Par. 0025, 0027) and generating a respective clock signal (master and various slave) for each of the boxes (Figure 3), Strong does not specifically show that the reference clock is defined by a plurality of communications protocol clock frequencies associated with the multi-protocol communications system.

Yu shows the reference clock is defined by a plurality of communications protocol clock frequencies associated with the multi-protocol communications system (Figure 1; col. 1, line 67 to col. 2, lines 9; generate a reference clock signal having a reference frequency for an electronic device from a base clock signal having a base frequency from a base clock signal source that is external to the electronic device. Because the base clock signal source is external to the electronic device, the base frequency of the base clock signal may vary depending on the base clock signal source.). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Strong to include the features of Yu in order to have a stable reference frequency despite possible variations in the base frequency of the base clock signal (col. 6, lines 18-21).

As to claim 16, modified Strong shows at least one of the link analyzers is configured to generate the reference clock (Strong: Par. 0042; The clock signal delivered to the box 220 is multiplied by the clock multiplier 228 and the multiplied clock signal from the clock multiplier drives the time stamp counters of the slave box 220.).

As to claim 17, modified Strong shows at least one of the link analyzers is configured to generate the trigger (Strong: Par. 0033; control signals include, but are not

limited to, a time stamp clock from the clock multiplier 106, a run/stop/trigger (RST) signal, a trigger out (TO) signal, and a state reset (SR) signal.).

As to claim 18, this claim is rejected for the same reasoning as set forth in the rejection of claim 2.

As to claim 20, Strong shows that in a multi-link protocol analyzer having a plurality of link analyzers that collectively represent a plurality of different communication protocols and corresponding clock frequencies, a method for processing data events associated with a multi-protocol communications system (Figure 1 and 2; Par. 0011-0013; abstract), the method comprising: transmitting a reference clock (abstract; the master box generates a clock signal that is adjusted and distributed to the slave boxes; Par. 0041-0042), the reference clock frequency being different from each of the communications protocol clock frequencies (Figure 1-3, each slave box has a clock multiplier that multiplies the clock signal from the master box; as shown in Figure 2-3, the boxes are in cascade fashion, and the clock signal passed from one box to another is multiplied by a factor which makes the clock different for each of the boxes (slaves and master); Par. 0041-0042); capturing a plurality of data events, the captured data events collectively representing a plurality of communications protocols (0011-0012; when a port is triggered, data at the port is captured and stored); and timestamping at least some of the captured data events, each timestamp being based upon the reference clock (abstract; The clock signal thus received by the slave boxes drives a clock multiplier that in turn drives the time stamp counters of the ports in the domains across the respective boxes. The time stamps of ports within a domain are

synchronized because they are driven by the clock signal from the master box; Par. 0009, 0011-12, 0042).

Even though Strong has shown that each box is associated with different protocols with corresponding frequencies (Par. 0025, 0027) and generating a respective clock signal (master and various slave) for each of the boxes (Figure 3), Strong does not specifically show that the reference clock frequency is based upon a plurality of communications protocol clock frequencies.

Yu shows the step of using the plurality of communications protocol clock frequencies as a basis for determining a frequency of a reference clock (Figure 1; col. 1, line 67 to col. 2, lines 9; generate a reference clock signal having a reference frequency for an electronic device from a base clock signal having a base frequency from a base clock signal source that is external to the electronic device. Because the base clock signal source is external to the electronic device, the base frequency of the base clock signal may vary depending on the base clock signal source.). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Strong to include the features of Yu in order to have a stable reference frequency despite possible variations in the base frequency of the base clock signal (col. 6, lines 18-21).

As to claims 21, 23, 24, and 25, these claims are rejected for the same reasoning as set forth in the rejection of claims 2, 9, 4, and 11, respectively.

As to claim 26, modified Strong shows the reference clock is transmitted by one of the link analyzers (Figure 2; Par. 0041-0043).

As to claims 27, 28 and 29, these claims are rejected for the same reasoning as set forth in the rejection of claims 5, 13 and 14, respectively.

As to claim 30, Strong shows a computer program product for implementing a method for processing data events associated with a multi-protocol communications system (abstract; Par. 0027, 0032), the computer program product comprising: a computer readable medium carrying computer executable instructions for performing the method, wherein the method comprises: capturing a plurality of data events, the captured data events collectively representing a plurality of communications protocols (Par. 0011-0012; when a port is triggered, data at the port is captured and stored); and timestamping at least some of the captured data events, each timestamp being based upon a reference clock having a frequency (abstract; The clock signal thus received by the slave boxes drives a clock multiplier that in turn drives the time stamp counters of the ports in the domains across the respective boxes. The time stamps of ports within a domain are synchronized because they are driven by the clock signal from the master box; Par. 0009, 0011-12, 0042).

Even though Strong has shown that each box is associated with different protocols with corresponding frequencies (Par. 0025, 0027) and generating a respective clock signal (master and various slave) for each of the boxes (Figure 3), Strong does not specifically show that the reference clock frequency is based upon a plurality of communications protocol clock frequencies.

Yu shows the step of using the plurality of communications protocol clock frequencies as a basis for determining a frequency of a reference clock (Figure 1; col. 1, line 67 to col. 2, lines 9; generate a reference clock signal having a reference frequency for an electronic device from a base clock signal having a base frequency from a base clock signal source that is external to the electronic device. Because the base clock signal source is external to the electronic device, the base frequency of the base clock signal may vary depending on the base clock signal source.). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Strong to include the features of Yu in order to have a stable reference frequency despite possible variations in the base frequency of the base clock signal (col. 6, lines 18-21).

As to claims 31, 33, 34 and 35, these claims are rejected for the same reasoning as set forth in the rejection of claims 2, 9, 4 and 11, respectively.

As to claim 36, modified Strong shows the data events captured in response the occurrence of a predetermined event (Strong: Par. 0017; when a port in a domain triggers or detects a predetermined condition or event, the port generates a trigger out signal that is provided to the master box through the control signals.).

As to claims 37, 38, 39 and 40, these claims are rejected for the same reasoning as set forth in the rejection of claims 5, 14, 6 and 13, respectively.

4. Claims 3, 8, 19, 22, 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strong (US 2004/0049706 A1; hereinafter Strong) in view of Yu et al.

(US 6,070,248; hereinafter Yu) in further view of Hansen et al. (US 6,269,136 B1; hereinafter Hansen).

As to claim 3, modified Strong shows all of the elements except a reference clock frequency that is higher than any of the plurality of communications protocol clock frequencies.

Hansen shows the a reference clock frequency that is higher than any of the plurality of communications protocol clock frequencies (figure 2; col. 3, lines 33-42; the communications clock has a frequency of N times the reference clock frequency and the master clock has a frequency of M times the reference clock frequency, where N<M.). It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the method of modified Strong to include the features of Hansen in order to synchronize bh request data streams and response data streams to the clock signal of the receiving device, which accomplishes the synchronization with minimal delay and maximum reliability (col. 1, lines 60-63).

As to claims 8, 19, 22, and 32, these claims are rejected using the same reasoning set forth in the rejection of claim 3.

Response to Arguments

5. Applicant's arguments, see Applicant's Remarks, filed January 09, 2008, with respect to the rejection(s) of claim(s) 1-40 under 35 USC 102(e) a being anticipated by Strong (US 2004/0049706) have been fully considered and are persuasive. Therefore,

the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made as shown in the above rejections.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 5,535,193	US 5,590,116
US 6,665,316 B1	US 6,370,159 B1
US 6,335,931 B1	US 7,173,943 B1

Any inquiry concerning this communication or earlier communications from the examiner should be directed to REDENTOR M. PASIA whose telephone number is (571)272-9745. The examiner can normally be reached on M-F 7:30am to 4:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Aung Moe can be reached on (571)272-7314. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aung S. Moe/
Supervisory Patent Examiner, Art Unit 2616

/Redentor M Pasia/
Examiner, Art Unit 2616